Technological Developments for THz Electronics

Chih-I Lin[1], Manuel Rodríguez-Gironés, Victoria Ichizli, Mustafa Saglam, P. Szeliga, Hans L. Hartnagel

Abstract **– Due to the lack of available power with raising frequencies, the quality and performance requirements on THz devices and circuits are especially high. Effects traditionally considered as secondary become unusually relevant and a great deal of research as well as very complex and demanding fabrication control processes are required to minimise them. In this paper we report on the recent technological efforts carried out at Darmstadt in the field of THz electronics in respect to devices as well as passive circuits elements.**

I. Introduction

For the submillimetre wavelength region, devices with high cut-off frequencies over 1 THz are key active elements for both mixing and multiplying applications. Pt/n-GaAs Schottky diodes have been proven to be the best-performing devices at room temperature up to several Terahertz. In order to increase the breakdown voltage of the diode, optimisation of the passivation technique was performed. To reduce the excess noise introduced by the reactive ion etching process during the anode opening process, an investigation on the etching parameters and on post-RIE treatment methods was undertaken. Back deposition of organic etching products onto the opened area, which result in inhomogeneous deposition of Pt/n-GaAs Schottky contact, was performed. Recently, heterostructure barrier varactors have shown significant improvement in tripler performance and could be a new challenge to Schottky varactor diodes for frequency multiplication applications. With increasing interest on integration of active devices and passive circuit elements, further technological developments were carried out, which include the micro-air-bridge technique, micro-lines for coplanar as well as microstrip waveguides.

II. Device Technologies

A. *Pt/n-GaAs Schottky Diode:*

The basic difference between whisker-contacted Schottky diodes and planar diodes is the usage of semiconductor area for the Schottky contact. This represents around 50% for whisker-contacted diodes and 0,2% for planar diodes. The situation is even worse for integrated circuits, where typically only one Schottky diode is realised over an area greater than 1 mm^2. Therefore, it is important to optimise the critical process steps in order to increase the yield of the Schottky contact. The critical steps directly related to the quality of the Schottky contact are the passivation and the anode opening using RIE.

1. *Passivation Technique:*

Unlike Silicon, GaAs can not be thermally oxidised on the surface to realise a good native passivation layer. Therefore, deposited SiO_2 is usually applied as the passivation layer. However, the SiO_2-layer results in a breakdown voltage of Pt/n-GaAs Schottky diode lower. The PECVD-technique can provide layers with different characteristics by combining process gases. In our investigation, we have changed the process parameters including the gas mixture, the process temperature and the process rf power. It is found that the gas flows and the rf power have the largest influence on the breakdown voltage of Schottky varactor diodes. Fig. 1 shows the dependence of the breakdown voltage on the N_2O gas flow while other gas flows are fixed to standard values. The influence of rf power is shown in Fig. 2.

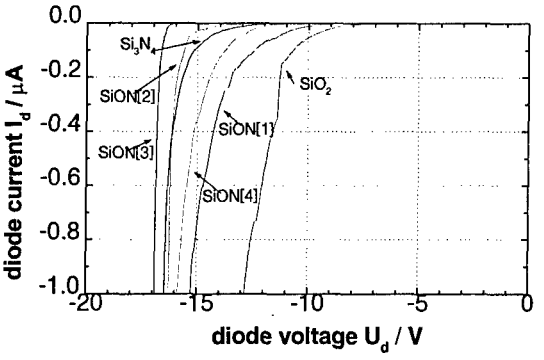

Fig.1: reverse I/V-characteristics of Schottky diodes with different passivation layers realised by changing gas mixture in the PECVD process.

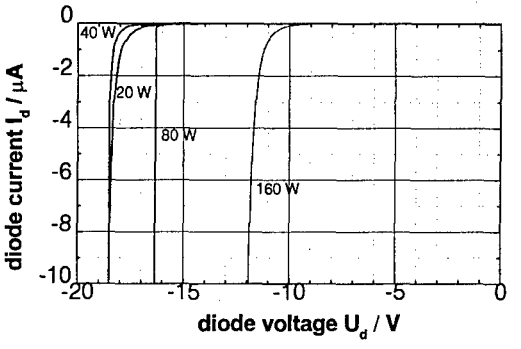

Fig.2: reverse I/V-characteristics of Schottky diodes with different passivation layers realised by varying process rf power.

[1] The authors are with the Institut für Hochfrequenztechnik, TU Darmstadt, Merckstrasse 25, D-64283 Darmstadt, Germany
E-Mail: hfmwe013@hrz2.hrz.tu-darmstadt.de
Home-Page: http://www.hf.e-technik.tu-darmstadt.de/thz.html

Both results indicate that proper passivation parameters have to be chosen to get the maximum value of breakdown voltages for given doping levels.

2. *Reduction of Excess Noise Resulted from Reactive Ion Etching:*
The reactive ion etching for Schottky contact area opening is the most critical step for the fabrication of Schottky diodes. It provide repeatable etch results and well-defined openings. Nevertheless, it introduces much higher excess noise which can degrade the rf performance of Schottky diodes. In our investigation, it is verified that a thermal treatment after RIE can reduce the noise temperature of Schottky diodes dramatically. Fig. 3 shows measured diode noise temperature at 1.5 GHz in dependence of overetching times. A 12-minute-ecthing is usually applied to exactly remove the passivation of the anode openings. One can notice that even with an overetching time of 15 minues, a comparable noise temperature curve can be achieved when a thermal treatment is applied to the overetched sample.

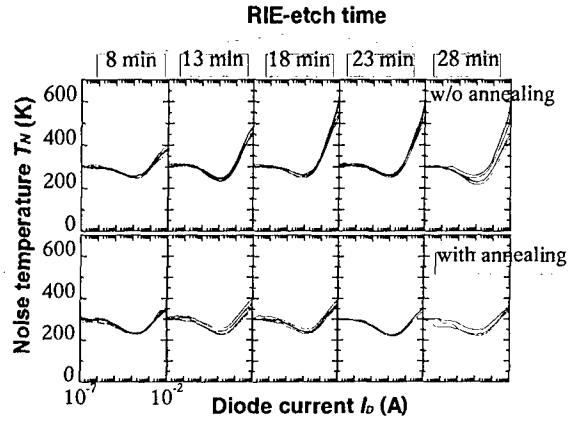

Fig. 3: Measured noise temperatures of test diodes with and without thermal treatment after the different RIE-etch times. 12 minutes of RIE are the minimum expected to remove the passivation layer.

3. Removal of Back Deposition resulting from RIE
Another disadvantage of RIE is the back deposition of etching products onto the surface which prevents homogeneous deposition of Schottky contacts and introduces a interface between the Schottky metal and the semiconductor. This layer can be effectively removed by applying AZ 400K developer directly after the RIE process. Fig. 4 shows a test sample before and after the cleaning process. Significant difference in the surface colour can be noticed.

B. *Heteros tructure Barrier Varactors (HBVs)*

The Heterostructure Barrier Varactor (HBV) is being recently intensively investigated for direct tripling since its C–V characteristic is evenly symmetric so that only odd harmonics are generated. Because it does not need any DC bias, it is very suitable for quasi-optical power combining system. Fig. 5 shows a SEM picture of an GaAs/AlGaAs-HBV chip after completing the process and Fig. 6 the measured C/V-characteristics using a network analyser at 1 GHz.

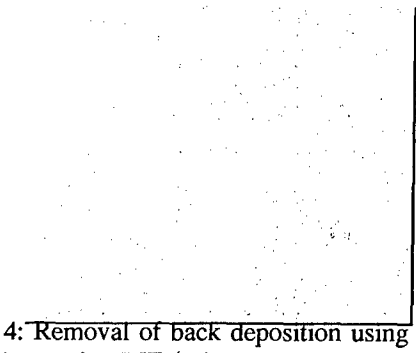

Fig. 4: Removal of back deposition using AZ400K developer after RIE (left / bottom: before treatment, right / top: after treatment).

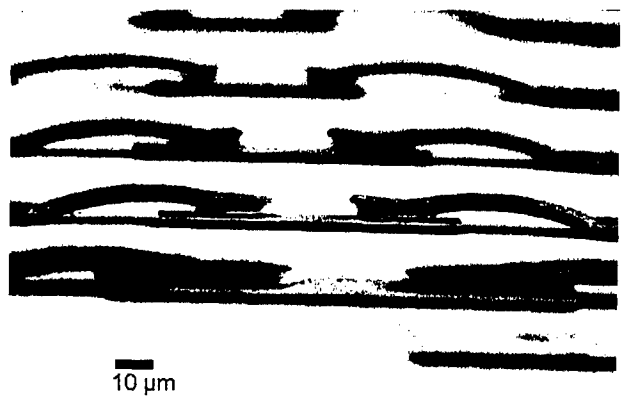

Fig. 5: SEM picture of a GaAs/AlGaAs-HBV chip after the fabrication process.

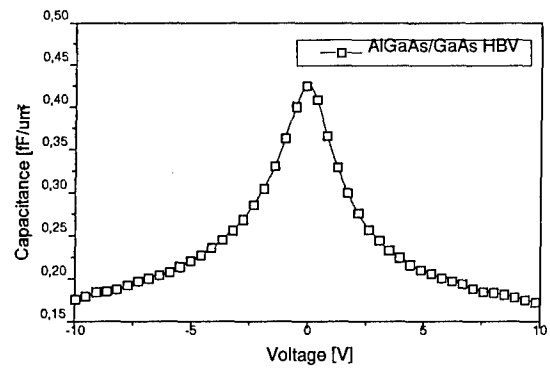

Fig. 6: at 1 GHz measured C/V-characteristics of an HBV

C. *Micro-Air-Bridge Optimisation*

For planar device technologies, a mechanically stable micro-air-bridge is as important as the diode itself. We have achieved high adhesion of electrolytically plated gold to a Pt/n-GaAs Schottky contact by seeding the Au layer with a sputtered Ni/Ag/Ni layer. After anode deposition and mesa formation, the needed air-bridge and pad shapes are defined photolithographically, a Ni(20nm)/Ag(80nm)/Ni(50nm) seed layer is deposited by sputtering. This enables a very dense, well-adhering layer which may be removed selectively to GaAs with different etchants. Optimisation of selective removal of this seed layer with presence of plated Gold was performed, in order to avoid large undercutting which can lead to

disconnection of the interconnects, contacting pads, etc. from the substrate. Fig. 7 shows the results achieved by the etching optimisation with minimum undercutting due to the high adhesion of the seed layer. This provides a high robustness of the micro air-bridge structure.

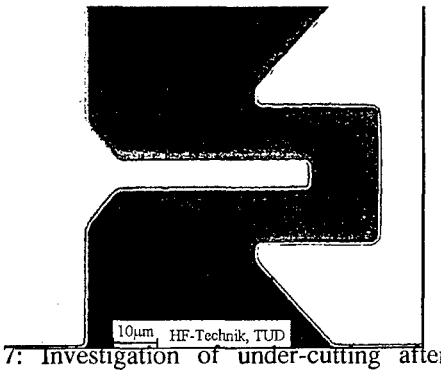

Fig. 7: Investigation of under-cutting after the process of the air-bridge. The under-cutting of the seed layer is about 1 µm.

III. Integration of THz Circuit Elements

In addition to the device developments, further technologies such as coplanar waveguides and microstrip waveguides are necessary for the monolithic integration. However, the devices as well as the circuit elements become electromagnetically large as the frequencies increase. Therefore, as opposed to the simulation and design technologies in the millimeter wave region with a relatively large tolerance in the design, sub-millimetre wave circuits have to be considered more carefully. Any discontinuity along the circuit lines can not be neglected. Therefore, 3-D electromagnetic simulators such as High Frequency Structure Simulator or Microwave Studio have to be applied to calculate their characteristics and transfer them into S-parameter for system performance optimisation. Some important technological aspects have been to be done to realise a stable fabrication process of monolithically integrated THz circuits:

1. Control of Metallisation Shape and Dimensions
   With the success of MMICs, the interest to realize SMMICs is getting larger. The dimension of passive elements in SMMICs must decrease, which means that the requirements on the precision of the fabrication is higher. In addition, in mixing applications, for example, the intermediate frequency is usually several GHz, which imposes a limitation to the thinness fo the metallisation (a few µm). Therefore, control of the metallisation dimensions to avoid parasitic effects resulting from any technological deviation is an important task while realizing SMMICs. Fig. 8 shows a comparison of realised 2µm thick, 12 µm wide Au-metallised coplanar waveguide from top side as well as the bottom side to the original mask. It can be seen that the bottom side is of the same width of the mask. The top side of the metallisation is about 1µm wider than the mask. Such variation limited by the photo-resist can be considered during the simulation phase to get a more precise performance prediction.

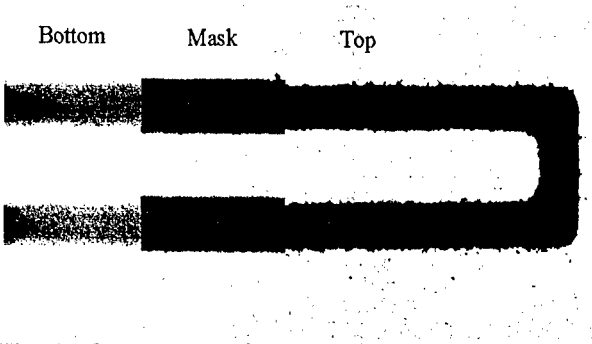

Fig. 8: Comparison of 2 µm thick Au-deposited coplanar waveguide from the top side and bottom side to the original mask. The original width of the middle line is of 6 µm. The bottom side has an identical width while the top side of about 1 µm wider than to the mask.

2. Thick Dielectrics for THz Circuits
   Dielectrics are necessary for circuits using microstrip, multi-layer and planarisation of planar and integrated devices. Dielectric layers with less mechanical stress, low loss at high frequencies, good adhesion and the technological possibility to realize via-hole contact are the main factors while when choosing a suitable dielectric layer. Fig. 9 illustrates a via-hole opening with a diameter of 3 µm to the Schottky diode through 5µm thick PECVD-deposited dielectrics.

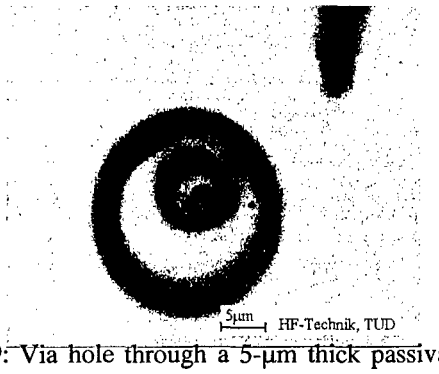

Fig. 9: Via hole through a 5-µm thick passivation layer. The 3-µm anode at the bottom of the via can be observed.

3. Process Control
   A large chip area over several mm^2 is usually used in monolithically integrated THz circuits. Therefore, it is important to introduce a system of process control for THz-device fabrication to make sure that the fabrication process is executed properly. In large series production, a system of Failure Mode, Effects and Criticality Analysis (FMECA) [1] is known representing a disciplined design review technique that focuses the development of products and processes on prioritised actions to reduce the risk of product field failures, and documents those actions and the review process in large series production. In opposite to FMECA, a small production which is nowadays typical for THz-electronics, needs a separate system of control and measures adjusted to its requirements. Such system of measures includes a process identification document (PID) and a lot-

traveller (LT) for each kind of device or circuit fabricated at TU Darmstadt. PID includes full description of the fabrication process, as well as complete guidelines for the technological facilities at TU Darmstadt necessary for the fabrication process. LT accompanies each sample batch (lot) during the whole technological process. All steps are recorded by the operator according to their date and time of performance. All changes of parameters are recorded and followed. All positive or optimised changes are introduced in the new version of LT for the following batch. Apart from that a thorough system of trouble shooting (TS) is developed. It increases device yield considerably. Both LT and TS contain many images illustrating the way structures should or should not look or behave themselves electrically. The documents and the process control system described above are the first known to be used at a research university that is active in small series-production in THz-electronics.

IV. Conclusion

In this paper, we present the recent technological developments of THz electronics at TU Darmstadt. Pt/n-GaAs Schottky diodes have been optimised with respect to applications in the frequency range 150-2500 GHz. An improved passivation technique and post-RIE treatment leads to a significant performance improvement in the diode characteristics. The optimisation of the micro-air-bridge, the metallisation techniques and the thick dielectrics along with the optimised device technique enables a precise fabrication of SMMICs.

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